REMARKS

The Office Action dated December 8, 2004 has been received and carefully considered. Claims 1-13 and 18-33 are pending. Claims 18 and 33 are allowed, claims 8 and 26 are objected to, and claims 1-7, 9-13, 19-25 and 27-32 are rejected. Reconsideration of the outstanding objections and rejections in the present application is respectfully requested in view of the following remarks.

Allowability of Claims 8, 18, 26 and 33

The Applicants note with appreciation the indication at page 8 of the Office Action that claims 18 and 33 are allowed and that claims 8 and 26 would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims. The Applicants have elected to forgo rewriting these claims in view of the following remarks.

Amendment of Claim 33

Claim 33 has been amended to provide proper antecedent support and not to narrow its scope.

Anticipation Rejections of Claims 1, 7, 19, 25 and 32

At page 2 of the Office Action, claims 1, 7, 19, 25 and 32 were rejected under 35 U.S.C. § 102(b) as being anticipated by Long (U.S. Patent No. 6,153,534). At page 3, claims 1, 7, 19, 25 and 32 were rejected under 35 U.S.C. § 102(b) as being anticipated by Xiang (U.S. Patent No. 6,200,863). These rejections are respectfully traversed.

Claim 1, from which claim 7 depends, recites, in part, the limitations of etching a dielectric spacer layer without the use of a sacrificial forming spacer to form L-shaped spacers for a gate structure, the L-shaped spacers including a first L-shaped spacer adjacent to a first sidewall of the gate structure and a second L-shaped spacer adjacent to a second sidewall of the gate structure. Claim 19, from which claim 25 depends, recites, in part, the limitations of forming a dielectric spacer layer over a semiconductor substrate having a first exposed surface portion adjacent a first sidewall of a gate structure and a second exposed surface portion adjacent a second sidewall of the gate structure and etching said first and second exposed surface portion portions of the dielectric spacer layer to form first and second L-shaped spacers for the gate structure. Claim 32 recites, in part, the limitations of forming a dielectric spacer layer over a

semiconductor substrate and etching said dielectric spacer layer, prior to forming any layer overlying the dielectric layer, to form L-shaped spacers for a gate structure, the L-shaped spacers including a first L-shaped spacer adjacent to a first sidewall of the gate structure and a second L-shaped spacer adjacent to a second sidewall of the gate structure.

With respect to these limitations, the Examiner asserts that Long discloses "forming a dielectric spacer layer (250) over the semiconductor substrate; and etching said dielectric spacer layer without the use of a sacrificial forming spacer, to [form] L-shape spacers. (figure 7a)" and makes specific reference to the passage of Long at col. 5, line 25 to col. 6, line 25. *Office Action*, p. 2. As for Xiang, the Examiner asserts that Xiang discloses "forming a dielectric spacer layer (24) over the semiconductor substrate; and etching said dielectric spacer layer without the use of a sacrificial forming spacer, to [form] L-shape spacers. (figure 4)." *Office Action*, p. 3. As noted in the response to the previous Office Action, neither Long nor Xiang disclose or suggest multiple L-shape spacers. Instead, as demonstrated by Figures 7A-8B of Long and Figures 4 and 5 of Xiang, both Long and Xiang teach only a single spacer. The Examiner admits that Long and Xiang fail to disclose or suggest two L-shape spacers, but asserts that "the courts have held that 'although the reference does not disclose a plurality of ribs, the court held that mere duplication of parts has no patentable significance unless a new and unexpected result is produced'" and makes reference to *In re Harza*, 274 F.2d 669, 124 U.S.P.Q. 378 (1960). *Office Action*, p. 9. The Applicants disagree and respectfully submit that the Examiner's reasoning is inconsistent with an anticipation rejection.

Anticipation under 35 U.S.C. § 102 requires that a prior art reference disclose, either expressly or under the principles of inherency, each and every element of the claimed invention. *In re Sun*, 31 USPQ2d 1451, 1453 (Fed. Cir. 1993) (unpublished). As admitted by the Examiner, neither Long nor Xiang expressly disclose two L-shape spacers, nor are two L-space spacers inherent to the teachings of Long or Xiang. Long expressly teaches one L-shape spacer on one side of the gate structure and a different shaped spacer on the opposing side of the gate structure. *See, e.g., Long*, Fig. 8A. Similarly, Xiang expressly teaches that only one spacer 28 is to be used to "mask a portion of the substrate adjacent to the drain edge of the gate electrode" so that "[h]eavily-doped source-drain extension regions [may be] formed in which the drain-side extension region is displaced away from the drain-side edge of the gate electrode by a distance equivalent to the lateral extend of the sidewall spacer." *Xiang*, Abstract. Thus, because the

limitations of two L-shape spacers is neither expressly disclosed or inherent to Long or Xiang, the Examiner has failed to establish that a prima facie anticipation rejection under 35 U.S.C. § 102.

Not only do Long and Xiang fail to anticipate claims 1, 7, 19, 25 and 32, the Examiner's proposed extension of the teachings of Long and Xiang to include multiple L-shape spacers is contrary to teachings of Long and Xiang and destroys the functionality of the inventions of Long and Xiang, and therefore is improper. Long teaches that

> [a]n aspect of the present invention also includes the step of implanting heavy ions into the spacer dielectric layer at an angle *such that the spacer dielectric layer at the drain side of the first material gate portion is substantially not implanted with the heavy ions. The spacer dielectric layer is then selectively etched such that any portion of the spacer dielectric layer that is implanted with the heavy ions is etched. Thus, the spacer dielectric layer on the drain side of the first material gate portion is not etched, but the spacer dielectric layer on the source side of the portion is etched.* In addition, an aspect of the present invention includes a step of *selectively growing a second material gate portion from the first material gate portion that is exposed on the source side of the first material gate portion.* In this manner, the dual material gate of the field effect transistor is comprised of the first material gate portion toward the drain of the field effect transistor and the second material gate portion toward the source of the field effect transistor.

Long, Abstract (emphasis added); *see also Id.*, col. 5, lines 44-53, col. 5, line 58 to col. 6, line 28; *see also Id.*, col. 6, lines 34-54 (teaching that the spacer dielectric layer 250 and the second material gate portion 280 are comprised of different materials and therefore cannot be etched from the same dielectric layer as recited by the claims).

Thus, as the above-cited passages demonstrate, Long teaches the formation of only a single spacer dielectric layer on the source side of a first material gate portion and the formation of a second material gate portion (but not a spacer) on the other side of the first material gate portion. The modification of the teachings of Long to include spacer dielectric layers on both sides of the first material gate portion as proposed by the Examiner not only lacks support in the disclosure of Long, but would prevent the formation of the second material gate portion and therefore would be counter to the specified goal of Long to fabricate "a dual material gate within a field effect transistor" such that "disadvantageous short channel effects are minimized." *Long*, col. 2, lines 22-25; *see also Id.*, Abstract.

Xiang teaches

> [a] A method for fabricating a semiconductor device having asymmetric source-drain extension regions includes the formation of a conformal layer of spacer forming material over a gate electrode. Nitrogen atoms are directionally introduced into the sidewall spacer material to form nitrogenated regions within the sidewall spacer material. The gate electrode casts a shadow over a portion of the sidewall spacer material adjacent to an edge of the gate electrode that is opposite from the direction of introduction of the nitrogen atoms. The shadow region of the sidewall spacer material remains free of nitrogen atoms. The shadow region of the sidewall spacer material is converted into a sidewall spacer by isotropically etching away the nitrogenated regions, while not substantially etching the shadow region. The asymmetrically formed sidewall spacer can then be used to mask a portion of the substrate adjacent to the drain edge of the gate electrode. Heavily-doped source-drain extension regions are formed in which the drain-side extension region is displaced away from the drain-side edge of the gate electrode by a distance equivalent to the lateral extent of the sidewall spacer. Upon removal of the sidewall spacer, a lightly-doped source-drain extension region is formed adjacent to the drain-side edge of the gate electrode.

Xiang, Abstract; *see also Id.*, col. 2, lines 38-63.

> As depicted in FIG. 5, sidewall spacer 28 blocks the implantation of dopant ions into the portion of p- region 14 directly beneath sidewall spacer 28. Accordingly, source-drain extension region 36 is offset from drain-side edge 30 of gate electrode 20 by a distance that is approximately equal to the lateral extent of sidewall spacer 28 overlying gate dielectric layer 18. *Additionally, the absence of a sidewall spacer adjacent to source-side edge 32 of gate electrode 20 results in the formation of source-drain extension region 34 in p- region 14 in spaced relation with source-side edge 32. By forming a relatively highly doped source-drain extension region near source-side edge 32, the series resistance of the MOS transistor remains low in the region of the transistor that does not contribute to hot carrier injection.*

Id., col. 5, lines 12-25 (emphasis added).

As the above-cited passages demonstrate, Xiang teaches the use of a single sidewall spacer 28 at the drain-side edge of the gate 20 to block implantation of dopant ions so as to offset the source-drain extension region 36 from the drain-side edge, while a spacer is intentionally omitted at the source-side edge of the gate electrode 20 so that "a relatively highly doped source-drain extension region" may be formed near the source-side edge to allow the series resistance of the MOS transistor to remain low "in the region of the transistor that does not contribute to hot carrier injection." *Id.* Thus, not only is the modification of the teachings of Xiang to include a second spacer opposite of the sidewall spacer 28 as proposed by the Examiner unsupported by

the disclosure of Xiang, the addition of such a second spacer would offset the source-drain extension region 34 away from the source-side edge and thus inhibit Xiang's specified goal of low series resistance in the region.

In view of the foregoing, it is respectfully submitted that the anticipation rejections of claims 1, 7, 19, 25 and 32 are improper at this time and withdrawal of these rejections therefore is respectfully requested.

Disqualification of Xiang as Prior Art in Obviousness Rejections

Xiang (U.S. Patent 6,200,863) is relied upon by the Examiner as prior art under 35 U.S.C. § 102(e) in a number of rejections of claims under 35 U.S.C. § 103(a). However, the invention of Xiang and the invention of the present application were under obligation of assignment to a common entity, namely Advanced Micro Devices, Inc. of Sunnyvale, California, at the times of their respective invention. Accordingly, the Applicants respectfully submit that Xiang is disqualified as prior art under 35 U.S.C. § 103(c) for the purpose of establishing obviousness rejections under 35 U.S.C. § 103(a).

Obviousness Rejection of Claims 2-6, 9-13, 20-24 and 27-31

At page 4 of the Office Action, claims 2-5 and 20-23 were rejected under 35 U.S.C. § 103(a) as being unpatentable over Long in view of Haskell (U.S. Patent No. 4,818,714). At page 5 of the Office Action, claims 2-5 and 20-23 were rejected under 35 U.S.C. § 103(a) as being unpatentable over Xiang in view of Haskell. At page 6 of the Office Action, claims 9-13 and 27-31 were rejected under 35 U.S.C. § 103(a) as being unpatentable over Long or Xiang in view of Nishizawa (U.S. Patent No. 6,613,686). At page 7 of the Office Action, claims 6 and 24 were rejected under 35 U.S.C. § 103(a) as being unpatentable over Long or Xiang in view of Verma (U.S. Patent No. 5,716,880). These rejections are respectfully traversed.

Claims 2-6 and 9-13 depend from claim 1, claims 20-24 and 27-32 depend from claim 19. As noted above, neither Long nor Xiang disclose or suggest the limitations of two L-shape spacers as recited by claims 1 and 19. The Office Action does not assert that Haskell, Nishizawa or Verma disclose or suggest these limitations. Accordingly the Office Action fails to establish that the proposed combinations of Long, Xiang, Haskell, Nishizawa and Verma dislose or suggest each and every limitation of claims 2-6, 9-13, 20-24 and 27-32 at least by virtue of their

dependency from one of claims 1 or 19. Moreover, these claims recite additional limitations neither disclosed nor suggested by the cited references. Additionally, as noted above, Xiang is not qualified prior art for the purposes of rejections under 35 U.S.C. § 103, so it is repectfully submitted that the Examiner's reliance on Xiang in the obviousness rejections is improper.

In view of the foregoing, it is respectfully submitted that the obviousness rejections of claims 2-6, 9-13, 20-24 and 27-32 are improper at this time and withdrawal of these rejections therefore is respectfully requested.

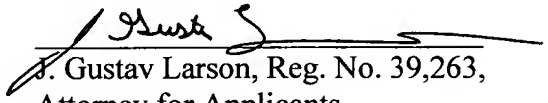
Conclusion

The Applicants respectfully submit that the present application is in condition for allowance, and an early indication of the same is courteously solicited. The Examiner is respectfully requested to contact the undersigned by telephone at the below listed telephone number in order to expedite resolution of any issues and to expedite passage of the present application to issue, if any comments, questions, or suggestions arise in connection with the present application.

The Commissioner is hereby authorized to charge any fees which may be required, or credit any overpayment, to Deposit Account Number 01-0365.

Respectfully submitted,

1-27-05
Date



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